Notice of References Cited	Application/Control No. 09/347,409	Applicant(s)/Patent Under Reexamination AKIMOTO ET AL.	
	Examiner Herng-der Day	Art Unit 2123	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-5,615,377	03-1997	Shimizu et al.	324/769
	B	US-5,974,247	10-1999	Yonezawa, Hirokazu	324/765
	C	US-6,047,247	04-2000	Iwanishi et al.	703/19
	D	US-6,278,964	08-2001	Fang et al.	703/14
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Quader et al., "Hot-carrier-reliability design guidelines for CMOS logic circuits", IEEE Journal of Solid-State Circuits, Volume 29, Issue 3, March 1994, pp 253-262
	V	Minehane et al., "Direct BSIM3v3 parameter extraction for hot-carrier reliability simulation of N-channel LDD MOSFETs", Proceedings of the 1997 6th International Symposium on Physical & Failure Analysis of Integrated Circuits, 1997, pp 133-139
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.